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Revision Lecture 2

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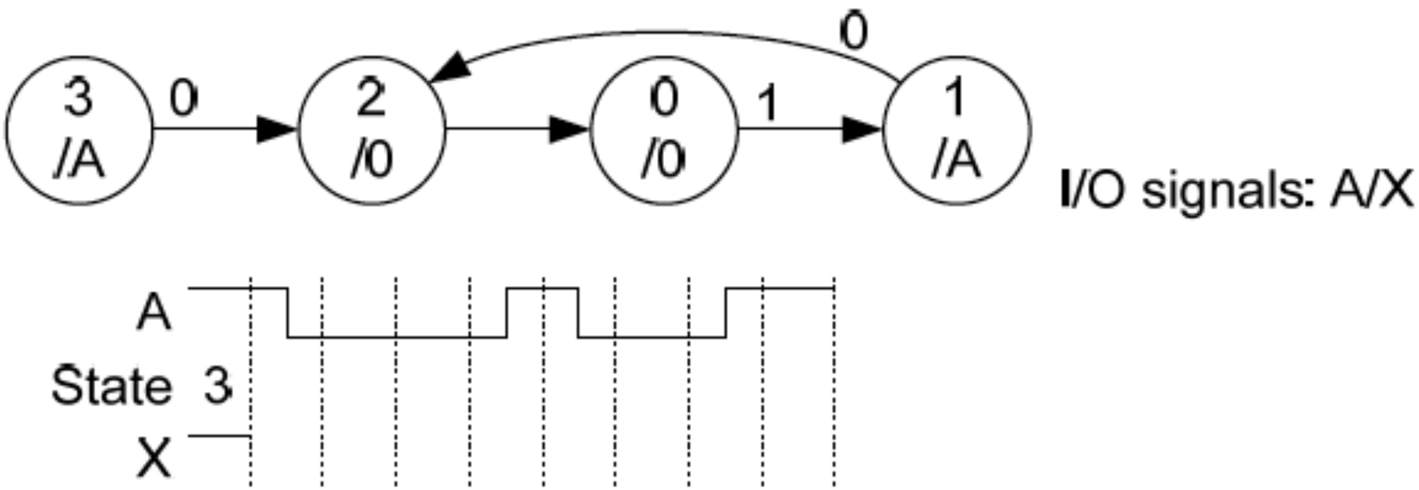
2010 Q1 (a) State Machine Analysis

Figure 1.1 shows the state diagram for a state machine with one input, A, and one output X. The state is represented by a 2-bit binary number in the range 0 to 3. The state changes only on the clock rising edges which are indicated by vertical dashed lines in the timing diagram.

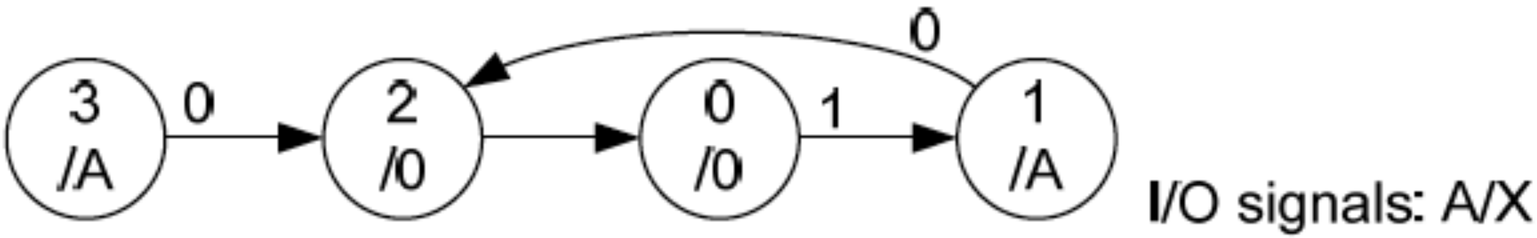
(i) Draw the state table for the state machine.

(ii) Complete the timing diagram showing the sequence of states taken and the waveform of the output X.



Q1 (a) Solution

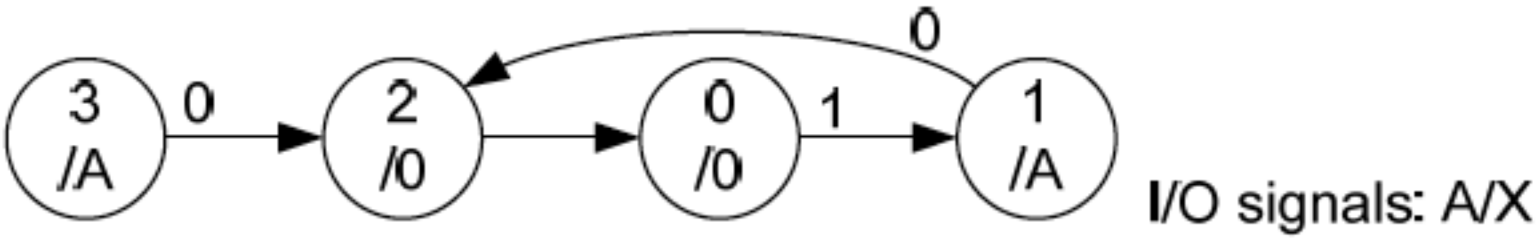
(i) Draw the state table for the state machine.

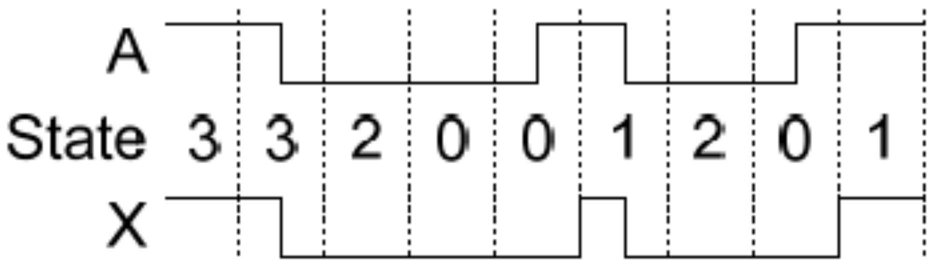


	NS1:0/X	A=0	A=1
S1:0	00	00/0	01/0
	01	10/0	01/1
	11	10/0	11/1
	10	00/0	00/0

Q1 (a) Solution

(ii) Complete the timing diagram showing the sequence of states taken and the waveform of the output X.



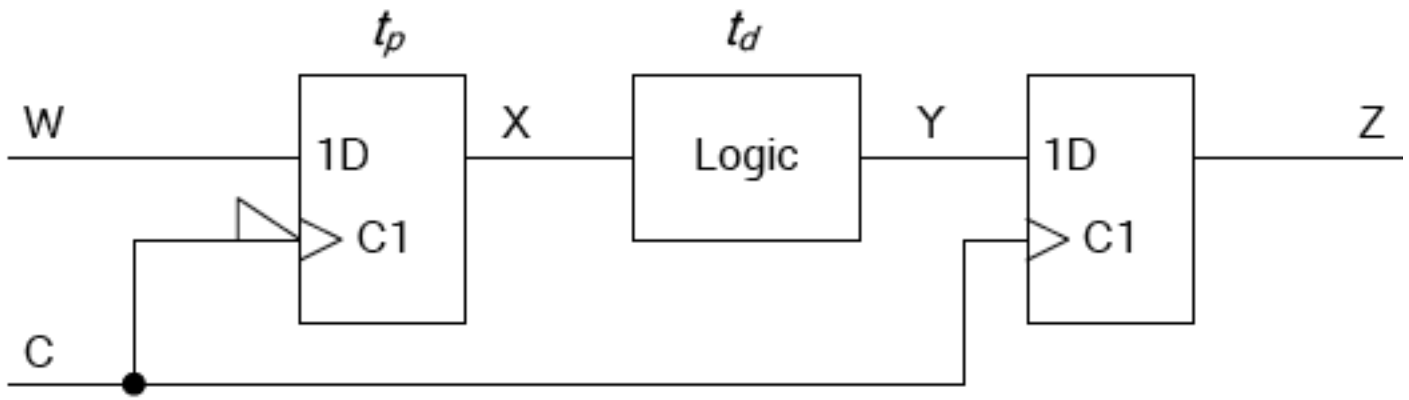


2009 Q1 (b) Timing

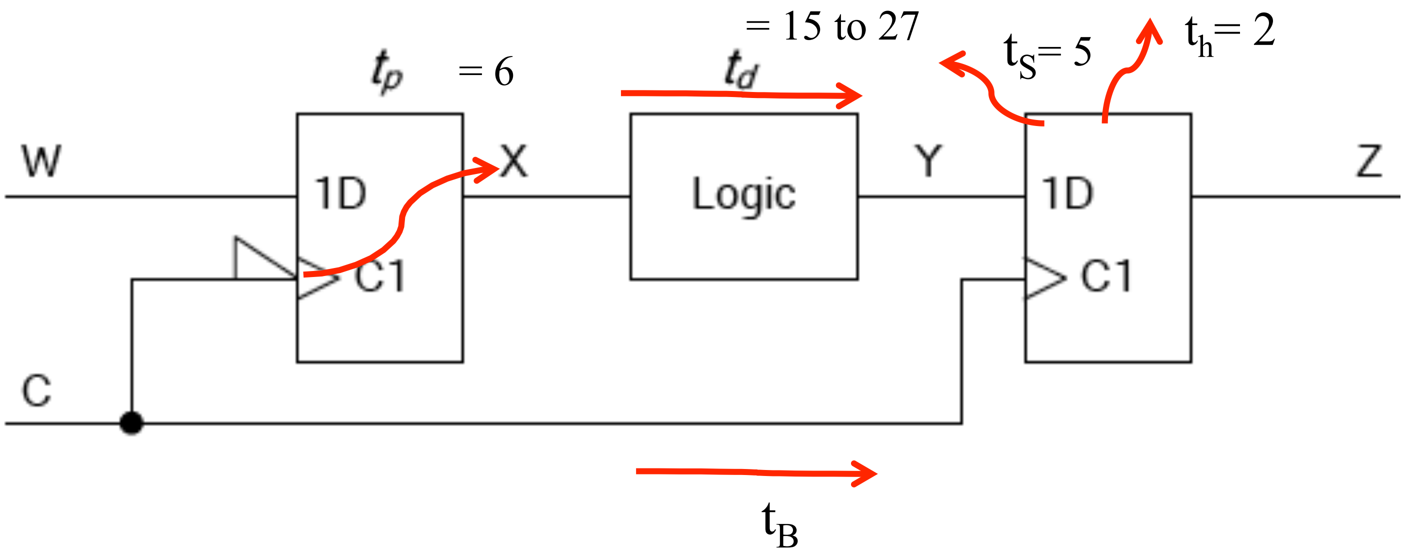
In the circuit of *Figure 1.2* the propagation delays of the leftmost flipflop and the logic block are t_p and t_d respectively. The rightmost flipflop has setup and hold times of t_s and t_h. The clock signal C is symmetrical with period T.

(i) Write the setup and hold inequalities that apply to the rightmost flip-flop.

(ii) Find the maximum clock frequency for the circuit if the timing parameters (in ns) are: $t_p = 6, t_s = 5, t_h = 2$ and $15 \le t_d \le 27$.



2009 Q1 (b) Solution



Taking a falling edge as the time reference, the setup equation is:

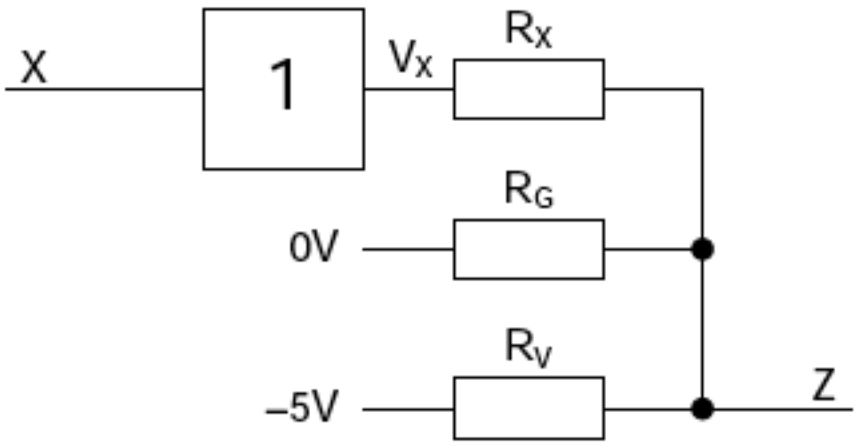
$$t_p + t_d + t_s < \tfrac{1}{2}T \quad \Rightarrow \quad 6 + 27 + 5 < \tfrac{1}{2}T \quad \Rightarrow \quad T > 76$$

The hold time equation is:

$$t_h < t_p + t_d + \tfrac{1}{2}T \quad \Rightarrow \quad 2 - 6 - 15 < \tfrac{1}{2}T \quad \Rightarrow \quad T > -38$$

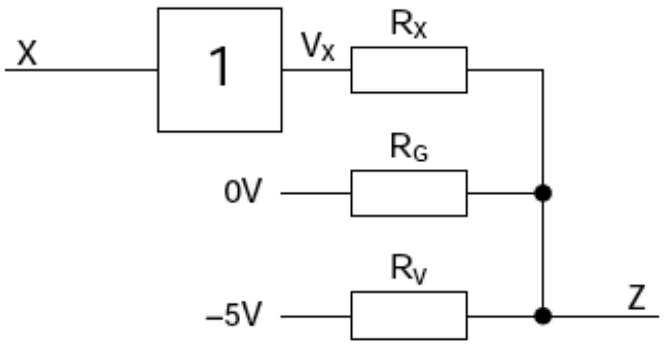
2010 Q1 (c) DAC

The gate output voltage, V_X, in *Figure 1.3* takes the values 0 and +5 V for logic zero and logic one respectively. Select the resistor values, R_X, R_G and R_V so that Z takes the values shown in the table and that the parallel combination of the three resistors equals 100 Ω.



X	Z
1	0.5 volts
0	-0.5 volts

2010 Q1 (c) Solution



Applying Kirchoff's current law at node Z gives:

X	Z
1	0.5 volts
0	-0.5 volts

$$Z = \frac{V_X R_X^{-1} - 5R_V^{-1}}{R_X^{-1} + R_G^{-1} + R_V^{-1}}$$

However, we know that the parallel combination of the resistors is 100 Ω, so the denominator equals 10 mS. Substituting for the given values of Z gives:

$$5R_X^{-1} - 5R_V^{-1} = 5\ \text{m}$$

$$-5R_V^{-1} = -5\ \text{m}$$

$$R_X^{-1} + R_G^{-1} + R_V^{-1} = 10\ \text{m}$$

From which we get $R_V = 1\ \text{k}\Omega$, $R_X = 500\ \Omega$ and $R_G = 143\ \Omega$.

2010 Q1 (d) Adder circuit

The circuit of *Figure 1.4* adds together two 3-bit unsigned numbers P2:0 and Q2:0 to give a 4-bit unsigned answer S3:0. The decimal values of P2:0, Q2:0 and S3:0 are denoted p, q and s respectively.

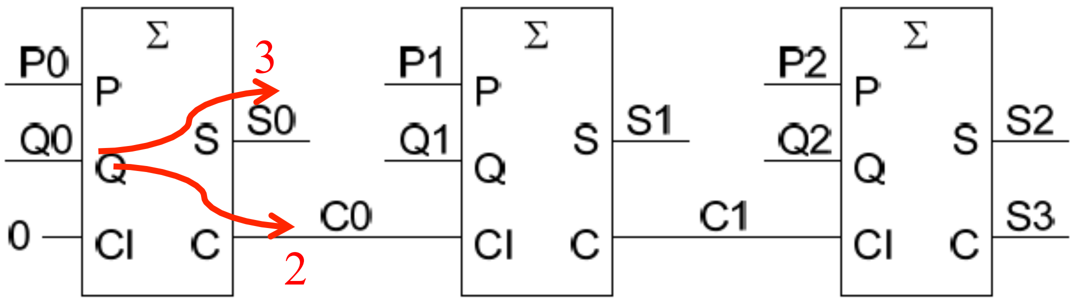
The propagation delays of the full adders to their S and C outputs are respectively 3 gate delays and 2 gate delays from any of their inputs.

Determine the longest propagation delay to any bit of S3:0 for each of the following cases:

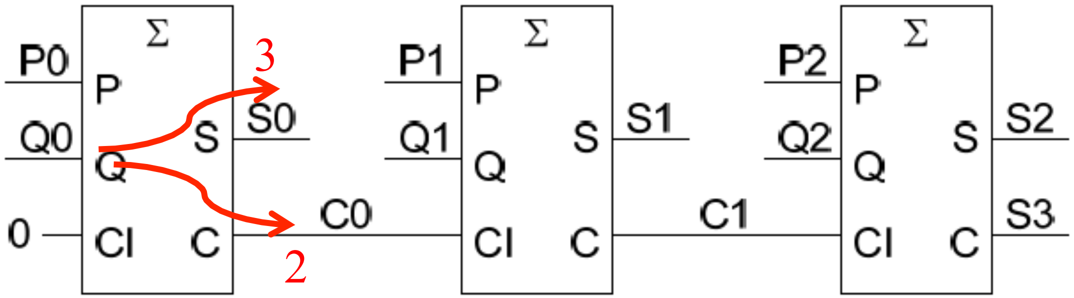
(i) Initially $p = 1$ and $q = 4$; then p changes to 2.

(ii) Initially $p = 1$ and $q = 7$; then p changes to 0.

(iii) Initially $p = 1$ and $q = 6$; then p changes to 2.



2010 Q1 (d) Solution



(i) Initially $p = 1$ and $q = 4$; then p changes to 2.

(ii) Initially $p = 1$ and $q = 7$; then p changes to 0.

(iii) Initially $p = 1$ and $q = 6$; then p changes to 2.

(i) s changes from 5 to 6 (0101 to 0110). All the carry signals remain at 0 throughout, so the delay is just 3 gate delays.

(ii) s changes from 8 to 7 (1000 to 0111). The longest delay path is P0-C0-C1-S2 which has a total delay of 7 gate delays.

(iii) s changes from 7 to 8 (0111 to 1000). The longest delay path is P1-C1-S2 which has a total delay of 5 gate delays.